IN THE CLAIMS:

Please cancel claim 1 and add claims 2-31 as follows:

2. An integrated circuit device, comprising:

a transmitter circuit including an output driver to synchronously output data with respect to a clock signal onto one or more external signal lines coupled to the transmitter circuit; and

a first register to store a first value representative of a transmit signal setting of the output driver, wherein the first value is determined in accordance with a configuration of one or more memory devices coupled to the one or more external signal lines and the transmit signal setting adjusts a transmit margin of the data.

3. The integrated circuit device of claim 2, wherein the transmit signal setting is selected from the group consisting of a high voltage level, a low voltage level, a reference voltage between the high voltage level and the low voltage level, a voltage asymmetry, a voltage swing, a current swing, a slew rate, an equalization setting to compensate for a residual signal on the one or more external signal lines, an equalization setting to compensate for a cross-coupled signal on the one or more external signal lines and a timing offset.

4. The integrated circuit device of claim 2, wherein the configuration is determined by accessing a supplemental memory device.

5. The integrated circuit memory device of claim 4, wherein the supplemental memory device comprises a serial presence detect memory device.

6. The integrated circuit memory device of claim 5, wherein the serial presence detect memory device is associated with a memory module coupled to the one or more external signal lines, wherein the memory module includes one or more memory devices.

7. The integrated circuit memory device of claim 2, wherein the integrated circuit device is configured to use a serial chain technique to determine the configuration of the one or more memory devices coupled to the one or more external signal lines, wherein positions of the one or memory devices on the one or more external signal lines are determined in order of closest to furthest from the integrated circuit device.

8. The integrated circuit device of claim 2, wherein the transmit margin comprises a voltage margin.

9. The integrated circuit device of claim 2, wherein the transmit margin comprises a timing margin.

10. The integrated circuit device of claim 2, wherein the configuration includes positions of one or more memory modules along the one or more external signal lines, the one or more memory modules including one or more memory devices.

11. The integrated circuit device of claim 2, wherein the configuration of the one or more memory devices includes positions of the one or more memory devices along the one or more external signal lines.

12. The integrated circuit device of claim 2, further comprising:

an input receiver coupled to the one or more external signal lines, wherein the input receiver samples data at a sample time with respect to the clock signal; and

a second register to store a second value representative of a receive signal setting of the input receiver, wherein the second value is determined in accordance with the configuration of the one or more memory devices coupled to the one or more external signal lines and the receive signal setting adjusts a receive margin of the data.

13. The integrated circuit device of claim 12, wherein the receive signal setting is selected from the group consisting of a high voltage level, a low voltage level, a reference voltage between the high voltage level and the low voltage level, a voltage asymmetry, a voltage swing, a threshold voltage, a current swing, a slew rate, an equalization setting to compensate for a residual signal on the one or more external signal lines, an equalization setting to compensate for a cross-coupled signal on the one or more external signal lines and a timing offset.

14. The integrated circuit device of claim 12, wherein the receive margin comprises a voltage margin.

15. The integrated circuit device of claim 12, wherein the receive margin comprises a timing margin.

16. A system comprising:

an integrated circuit device, the integrated circuit device including:

a first transmitter circuit including a first output driver to synchronously output data with respect to a first clock signal onto one or more external signal lines coupled to the first transmitter circuit; and

a first register to store a first value representative of a transmit signal setting of the first output driver, wherein the first value is determined in accordance with a configuration of one or more memory devices coupled to the one or more external signal lines and the transmit signal setting of the first output driver adjusts a transmit margin of the data; and

a memory device coupled to the one or more external signal lines, the memory device including:

a first input receiver, wherein the first input receiver samples data at a sample time with respect to a second clock signal; and

a second register to store a second value representative of a receive signal setting of the first input receiver, wherein the second value is determined in accordance with a configuration of the memory device and the integrated circuit device, and the receive signal setting of the first input receiver adjusts a receive margin of the data.

17. The system of claim 16, wherein the transmit signal setting of the first output driver is selected from the group consisting of a high voltage level, a low voltage level, a reference voltage between the high voltage level and the low voltage level, a voltage asymmetry, a voltage swing, a current swing, a slew rate, an equalization setting to compensate for a residual signal on the one or more external signal lines, an equalization setting to compensate for a cross-coupled signal on the one or more external signal lines and a timing offset.

18. The system of claim 16, wherein the configuration of the memory device is determined by accessing a supplemental memory device.

19. The system of claim 18, wherein the supplemental memory device comprises a serial presence detect memory device in the memory device.

20. The system of claim 16, wherein the transmit margin comprises a voltage margin.

21. The system of claim 16, wherein the transmit margin comprises a timing margin.

22. The system of claim 16, wherein the first value in the first register and the second value in the second register are complementary to one another such that increased margin

associated with the transmit signal setting of the first output driver and the receive signal setting of the first input receiver do not substantially duplicate one another.

23. The system of claim 16, wherein the receive signal setting of the first input receiver is selected from the group consisting of a high voltage level, a low voltage level, a reference voltage between the high voltage level and the low voltage level, a voltage asymmetry, a voltage swing, a threshold voltage, a current swing, a slew rate, an equalization setting to compensate for a residual signal on the one or more external signal lines, an equalization setting to compensate for a cross-coupled signal on the one or more external signal lines and a timing offset.

24. The system of claim 16, wherein the receive margin comprises a voltage margin.

25. The system of claim 16, wherein the receive margin comprises a timing margin.

26. The system of claim 16, wherein the configuration comprises a position of the memory device along the one or more external signal lines.

27. The system of claim 16, the memory device further including:

a second transmitter circuit including a second output driver to synchronously output data with respect to the second clock signal onto the one or more external signal lines coupled to the second transmitter circuit; and

a third register to store a third value representative of a transmit signal setting of the second output driver, wherein the third value is determined in accordance with the configuration of the memory devices and the integrated circuit device, and the transmit signal setting of the second output driver adjusts the transmit margin of the data.

28. The system of claim 27, wherein the transmit signal setting of the second output driver is selected from the group consisting of a high voltage level, a low voltage level, a reference voltage between the high voltage level and the low voltage level, a voltage asymmetry, a voltage swing, a current swing, a slew rate, an equalization setting to compensate for a residual signal on the one or more external signal lines, an equalization setting to compensate for a cross-coupled signal on the one or more external signal lines and a timing offset.

29. The system of claim 27, the integrated circuit device further including:

a second input receiver, wherein the second input receiver samples data at a sample time with respect to the first clock signal; and

a fourth register to store a fourth value representative of a receive signal setting of the second input receiver, wherein the fourth value is determined in accordance with a configuration of the memory device and the integrated circuit device, and the receive signal setting of the second input receiver adjusts the receive margin of the data.

30. The system of claim 29, wherein the receive signal setting of the second input receiver is selected from the group consisting of a high voltage level, a low voltage level, a reference voltage between the high voltage level and the low voltage level, a voltage asymmetry, a voltage swing, a threshold voltage, a current swing, a slew rate, an equalization setting to compensate for a residual signal on the one or more external signal lines, an equalization setting to compensate for a cross-coupled signal on the one or more external signal lines and a timing offset.

31. The system of claim 29, wherein the third value in the third register and the fourth value in the fourth register are complementary to one another such that increased margin associated with the transmit signal setting of the second output driver and the receive signal setting of the second input receiver do not substantially duplicate one another.